26. A memory device according to claim 15 including a substrate and configured so that the charge storage node is formed overlying the substrate, the barrier structure overlies the charge storage node, and the electrode structure overlies the barrier structure.

27. A memory device according to claim 26 including an insulating layer overlying the substrate, the charge storage node, barrier structure and the electrode structure overlying the insulating layer.

28. A memory device according to claim 27 including further device features formed in the substrate, the further device features underlying the insulating layer.

29. A memory device according to claim 27 wherein the insulating layer comprises an oxide of the material of the substrate.

30. A memory device according to claim 27 wherein the insulating layer extends over side edges of the barrier structure and the charge storage node.

31. A memory device according to claim 26 wherein the barrier structure is substantially co-extensive with the charge storage node.

32. A memory device according to claim 15 wherein the barrier structure has a material composition that provides an internal relatively high internal electrostatic barrier in the absence of an applied voltage to the electrode structure, whereby the electrostatic barrier can be lowered upon application of the external bias to the electrode structure.

33. A memory device according to claim 27 including a gate configured to apply said external bias into the barrier structure selectively to control conduction of charge carriers between the electrode structure and the charge storage node.

34. A memory device according to claim 15 wherein the charge storage node is made of conductive silicon material.

35. A method of fabricating a memory device, comprising: forming a charge storage node, an electrode structure and a barrier structure so that the barrier structure is disposed between the electrode structure and the charge storage node, and such that the barrier structure presents an internal relatively high electrostatic barrier potential that retains charge on the storage node, the barrier being lowerable by an external voltage applied to the electrode structure to allow charge transfer to and from the storage node.

36. A method of fabricating memory device according to claim 35 including providing a substrate, forming an electrically insulating layer on the substrate, forming the charge storage node overlying the insulating layer, forming the barrier structure so as to overlie the charge storage node, and providing the electrode structure overlying the barrier structure.

37. A method according to claim 35 including oxidising the substrate to form the insulating layer.

38. A memory device fabricated by a method according to claim 35

39. A device according to claim 21 including refresh circuitry to refresh the level of charge stored on the charge storage nodes individually.

40. A device according to claim 21 including reading circuitry to read the level of charge stored on the charge storage nodes of the cells individually.

41. A device according to claim 21 including writing circuitry to write charge to the charge storage nodes of the cells individually.

42. A memory device according to claim 21 wherein the barrier structure is formed of crystalline material.

43. A memory device according to claim 21 wherein the barrier structure includes polycrystalline silicon.

44. A memory device according to claim 21 wherein each of the memory cells includes a gate to apply said external bias to the barrier structure.

45. A memory device comprising
a substrate,
an array of memory cells configured on the substrate,
a plurality of word lines and data lines extending between the cells,
each of the memory cells comprising a charge storage node, an electrode coupled to one of the data lines and a barrier structure between the electrode and the charge storage node, the barrier structure providing an internal electrostatic barrier potential of a relatively high barrier height to store charge carriers on the charge storage node the barrier being configurable selectively in response to an external bias applied to one of the

word lines to provide a relatively low barrier height for which charge carriers can pass between the electrode structure and the charge storage node,

reading circuitry to read the level of charge stored on the charge storage nodes of the cells individually, and

writing circuitry to write charge onto the charge storage nodes of the cells individually.

46. A memory device according to claim 45 including an electrically insulating layer on the substrate with the array of memory cells overlying the insulating layer.

47. A memory device according to claim 45 wherein the substrate is comprised of silicon, the insulating layer is selected from a group comprising an oxide and a nitride of silicon, the charge storage node is formed of a conductive silicon material and the barrier structure is formed of polysilicon material.

48. A method of fabricating a semiconductor device, comprising: providing a substrate, forming device features in the substrate, forming an electrically insulating layer on the substrate overlying the device features, forming a charge storage node overlying the insulating layer, forming a barrier structure so as to overlie the charge storage node, and providing an electrode structure overlying the barrier structure, the barrier structure presenting an electrostatic barrier potential that retains charge on the storage node, the barrier being raisable and lowerable by an external voltage applied to the device so as to allow charge transfer to and from the storage node.

49. A method of fabricating a memory device comprising:
providing a substrate,

forming on the substrate an array of memory cells, a plurality of word lines and a plurality of data lines extending between the cells, each of the memory cells comprising a charge storage node, an electrode coupled to one of the data lines and a barrier structure between the electrode and the charge storage node, the barrier structure providing an internal electrostatic barrier potential with a relatively high barrier height to store charge carriers on the charge storage node the barrier potential being configurable selectively in response to an external bias applied to one of the word lines to provide a relatively low